

# Low-Loss CPW on Low-Resistivity Si Substrates with a Micromachined Polyimide Interface Layer for RFIC Interconnects

George E. Ponchak, *Senior Member, IEEE*, Alexandros Margomenos, *Member, IEEE*, and Linda P. B. Katehi, *Fellow, IEEE*

**Abstract**—The measured and calculated propagation constant of coplanar waveguide (CPW) on low-resistivity silicon ( $1 \Omega \cdot \text{cm}$ ) with a micromachined polyimide interface layer is presented in this paper. With this new structure, the attenuation (decibels per centimeter) of narrow CPW lines on low-resistivity silicon is comparable to the attenuation of narrow CPW lines on high-resistivity silicon. To achieve these results, a  $20\text{-}\mu\text{m}$ -thick polyimide interface layer is used between the CPW and the Si substrate with the polyimide etched from the CPW slots. Only a single thin-film metal layer is used in this paper, but the technology supports multiple thick metal layers that will further lower the attenuation. These new micromachined CPW lines have a measured effective permittivity of 1.3. Design rules are presented from measured characteristics and finite-element method analysis to estimate the required polyimide thickness for a given CPW geometry.

**Index Terms**—Attenuation, coplanar waveguide, interconnects.

## I. INTRODUCTION

THE possibility of low-cost radio-frequency integrated circuits (RFICs) integrated with digital circuitry is creating strong interest in silicon as a microwave substrate [1]–[4]. This is being driven by the development of SiGe heterojunction bipolar transistors (HBTs) with a maximum frequency of oscillation  $f_{\text{max}}$  of 160 GHz [5]. However, transmission lines and passive circuit components on standard low-resistivity silicon substrates such as used in CMOS processing have high loss. To overcome this problem, two approaches have been used for Si RFICs.

The more straightforward approach is to use high-resistivity silicon (HRS) substrates, resistivity greater than  $2500 \Omega \cdot \text{cm}$  [1], [2]. HRS has the advantage that transmission lines and passive components printed on it behave similarly to the same components on GaAs or other good microwave substrates. Thus, circuit designers may use the equivalent-circuit models and fabrication processes already available. However, HRS wafers are more expensive than standard silicon substrates and require modifications to standard CMOS fabrication processes.

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G. E. Ponchak is with the NASA Glenn Research Center, Cleveland, OH 44135 USA.

A. Margomenos and L. P. B. Katehi are with the Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109 USA.

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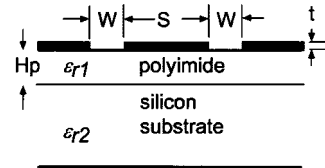


Fig. 1. Schematic of CPW line on low-resistivity Si wafer with a polyimide interface layer.

Both of these facts increase the cost of Si RFICs on HRS compared to standard CMOS circuits.

The other approach for Si RFICs is to use the polyimide layers, as used in CMOS processing for wafer planarization, to develop novel RF transmission lines on CMOS-grade Si substrates [3], [4]. For example, thin film microstrip (TFMS) is created by depositing a ground plane on the top side of the Si substrate, depositing a polyimide layer over it, and defining the strip on the top surface. Since the ground plane completely shields the electromagnetic fields from the lossy silicon wafer, low attenuation is possible with a polyimide less than  $10\text{-}\mu\text{m}$  thick [6]. Furthermore, since via holes are easily etched through the polyimide, multilayer interconnects are possible.

Microwave circuit designers often prefer a coplanar waveguide (CPW) because of its advantages in circuit layout that result from having the strip and the ground planes on the same surface. It has been shown that a CPW on low-resistivity silicon wafers with a polyimide interface layer, as shown in Fig. 1, can yield acceptable attenuation. However, since the interaction of the electromagnetic fields with the silicon substrate must be minimized for low loss, the polyimide thickness must be thicker than that for TFMS lines [7]. Alternatively, if the processing does not support thick polyimide, thick  $\text{SiO}_2$  may be used [8].

In this paper, experimental measurements and three-dimensional finite-element method (3-D-FEM) analysis are used to demonstrate that wave attenuation in CPW lines on a polyimide interface layer, such as shown in Fig. 1, is significantly reduced by etching the polyimide in the slot regions in a similar manner as is done for CPW lines on HRS [9], [10]. This lowers the effective dielectric constant, line capacitance, and current density, which leads to lower conductor loss. Besides lowering the attenuation per unit length, a very low effective dielectric constant has been measured and is reported here. Finally, design rules to determine the minimum polyimide thickness for low attenuation is presented.

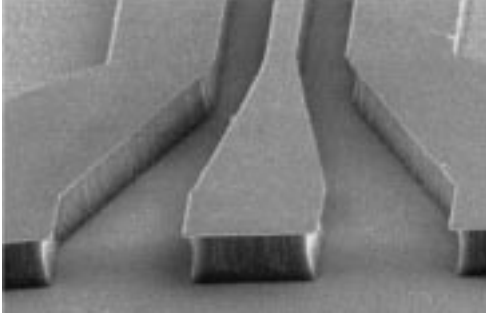


Fig. 2. SEM of micromachined CPW line on low-resistivity Si wafer with a polyimide interface layer ( $H_p = 20.15 \mu\text{m}$ ) that has been etched.

## II. FABRICATION AND TEST PROCEDURES

On four 385- $\mu\text{m}$ -thick  $1\text{-}\Omega\cdot\text{cm}$  silicon wafers, DuPont WE 1111 (now called PI-1111) polyimide is deposited and cured to a thickness  $H_p$  of 6.35, 8.83, 14.59, and 20.15  $\mu\text{m}$ . Sets of 15 different CPWs are fabricated on top of the polyimide using standard liftoff processing with the CPW made of 0.02  $\mu\text{m}$  of Ti and 1.5  $\mu\text{m}$  of Au. At this point, the transmission lines appear as shown in Fig. 1, where the polyimide not protected by the CPW metallization is removed by reactive ion etching (RIE) to obtain the structure shown in Fig. 2. No backside ground plane or Si passivation layers are grown, and WE1111 polyimide has a relative dielectric constant  $\epsilon_{r1}$  of 2.8.

The CPW propagation characteristics are measured with a vector network analyzer and probe station. A quartz spacer between the Si substrate and the probe station wafer chuck is used to eliminate parasitic microstrip and parallel-plate waveguide modes. The propagation constant  $\gamma = \alpha + j\omega\sqrt{\epsilon_{\text{eff}}}/c$ , where  $\alpha$  is the attenuation constant,  $\omega$  is the angular frequency,  $c$  is the velocity of light in vacuum, and  $\epsilon_{\text{eff}}$  is the effective dielectric constant, is deembedded through the thru-reflect-line (TRL) calibration routine implemented in the software program MULTICAL [11]. For each CPW line characterized, four delay lines with the longest line being 1 cm are used in addition to the thru line to enhance accuracy from 1 to 40 GHz.

The micromachined CPW lines are theoretically analyzed using a 3-D-FEM analysis implemented through Ansoft's high-frequency structure simulator (HFSS). The simulated structure is the same as the actual structure described above and is shown in Fig. 2, including the 2- $\mu\text{m}$  polyimide undercut of the CPW lines. Furthermore, to achieve good match between the measured and theoretical results, the Si wafer loss tangent of 0.0018 [12], the Si wafer resistivity, and the metal resistivity were used in the model. Radiation boundaries are used on the top and sides of the simulated structure.

## III. RESULTS

The attenuation in decibels per centimeter of three CPW lines after polyimide etch with  $H_p = 20.15 \mu\text{m}$  is shown in Fig. 3. At low frequency, below X-band, wider CPW lines have lower loss than narrow lines; however, the high-frequency behavior is not easily predicted. It is seen in Fig. 3 that the frequency dependence  $n$  of  $\alpha = a f^n$  varies with the strip and slot widths. Specifically, for narrow lines, the attenuation is conductor-loss dom-

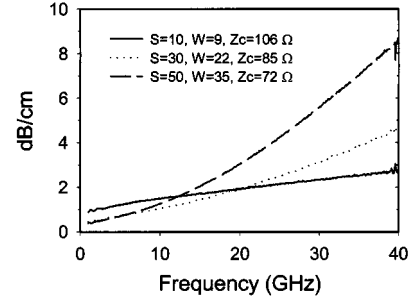


Fig. 3. Measured attenuation of micromachined CPW lines with  $H_p = 20.15 \mu\text{m}$ .

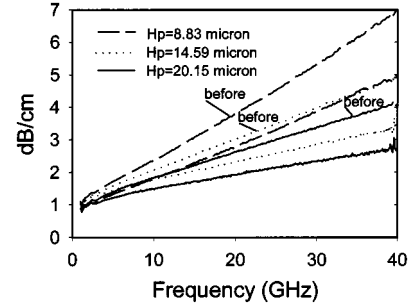


Fig. 4. Measured attenuation of CPW lines ( $S = 10$  and  $W = 9 \mu\text{m}$ ) before and after polyimide etch.

inated and varies as  $f^{0.5}$ , while for wider lines, the frequency dependence  $n$  increases to 1.5. Therefore, at high frequency, narrower CPW lines on polyimide have lower attenuation than wider lines. This is contrary to the attenuation characteristics of CPW lines on insulating substrates, which are dominated by conductor loss for both narrow and wide lines [13]. Note that, in Fig. 3, the lowest attenuation at 40 GHz is 2.75 dB/cm for a line with  $S$  and  $W$  of 10 and 9  $\mu\text{m}$ , respectively.

Fig. 4 shows the reduction in attenuation after etching the polyimide from the slots of three CPW lines with  $S$  and  $W$  of 10 and 9  $\mu\text{m}$ , respectively, on polyimide of thickness 8.83, 14.59, and 20.15  $\mu\text{m}$ . Note that each graph on Fig. 4 is for a different polyimide thickness and the upper line, indicating higher loss, is the attenuation of the CPW before polyimide etch. At 40 GHz, there is a 28% reduction in attenuation after etching for the CPW on the thinnest polyimide and a 35% reduction in attenuation for the CPW on the thickest polyimide. It is interesting that this reduction in attenuation is similar to the reduction in attenuation of CPW lines on HRS when the silicon is etched from the slots [9], [10].

The effective permittivity of the CPW lines after etching the polyimide also varies with the line geometry. If the approximate, but usually very accurate, estimate of  $\epsilon_{\text{eff}} = (\epsilon_r + 1)/2$  is used,  $\epsilon_{\text{eff}}$  should equal 1.9 for the CPW lines before the polyimide is etched if none of the fields interact with the silicon since  $\epsilon_r = \epsilon_{r1} = 2.8$ . Furthermore, the more the electric fields interact with the Si substrate, the higher  $\epsilon_{\text{eff}}$  will be. After the polyimide is etched and more of the fields are in air, both above the polyimide and in the slot region,  $\epsilon_{\text{eff}}$  should be less than 1.9. Fig. 5 shows the measured and calculated  $\epsilon_{\text{eff}}$  as a function of frequency for a narrow and a wide CPW line before and after the polyimide etch. There is excellent agreement between the

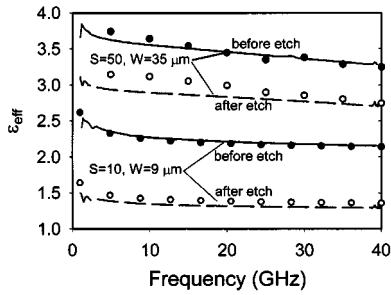


Fig. 5. Measured and calculated effective permittivity of micromachined CPW lines with  $H_p = 20.15 \mu\text{m}$ . Measured data is shown as lines and the calculated data is shown as discrete points.

measured and calculated values, which indicates the accuracy of both methods. The small difference between the two sets of values is attributed to difficulty in describing the physical structure used in modeling. Before the polyimide is etched,  $\epsilon_{\text{eff}}$  is greater than 1.9 for both CPW lines, indicating that the electric fields are still interacting with the Si. Etching the polyimide from the slots reduces  $\epsilon_{\text{eff}}$  by 17% for the wide CPW line and 36% for the narrow CPW line at 40 GHz. This percentage reduction in  $\epsilon_{\text{eff}}$  for the narrow CPW line is approximately the same as the percentage reduction in attenuation, as shown in Fig. 4. Lastly, note the narrow line has a very low  $\epsilon_{\text{eff}}$  of 1.3.

While low  $\epsilon_{\text{eff}}$  increases the circuit speed, it also makes it difficult to fabricate low characteristic impedance  $Z_c$  transmission lines since  $Z_c = A/\sqrt{\epsilon_{\text{eff}}}$  where  $A$  is only dependent on  $S$  and  $W$ . Based on the calculated  $Z_c$  of CPW lines on HRS and the measured  $\epsilon_{\text{eff}}$  of CPW lines on the micromachined polyimide,  $Z_c$  of the new CPW lines presented in this paper may be determined. This has been done for the three lines in Fig. 3, which have a characteristic impedance of  $50 \Omega$  on HRS. After etching the polyimide,  $Z_c$  is 106, 85, and  $72 \Omega$  for the CPW lines with  $S = 10, 30$ , and  $50 \mu\text{m}$  respectively, or  $Z_c$  of the new CPW lines presented here has increased by 112%, 70%, and 44%, respectively.

It was speculated above that the magnitude of the electric field in the silicon after etching is significantly lower, especially for narrow CPW lines. Using the 3-D-FEM analysis, the reduction in loss and effective permittivity is clearly shown to be due to a reduction in the electric fields in the Si wafer. Fig. 6(a)–(c) show the magnitude of the electric field in a cross-sectional cut through CPW lines with  $S = 50 \mu\text{m}$ ,  $W = 35 \mu\text{m}$ , and  $H_p = 8, 20$ , and  $50 \mu\text{m}$ , respectively. It is seen that the electric fields are concentrated along the metal edges of the CPW slots, and the field magnitude in the Si decreases as  $H_p$  increases. Note the darker colors in the polyimide under the CPW center strip for the thicker polyimide indicates lower field magnitude. The maximum electric field in the Si substrate for micromachined CPW lines with  $S$  and  $W$  of 50 and  $35 \mu\text{m}$  and 10 and  $9 \mu\text{m}$  as a function of  $H_p$  is presented in Fig. 7. It is seen that the maximum electric field in the Si is significantly lower for narrow CPW lines compared to wide CPW lines. In fact, for the  $20.15\text{-}\mu\text{m}$ -thick polyimide used in Fig. 5, the magnitude of the electric field in the Si is approximately 7.5 dB lower for the narrow CPW.

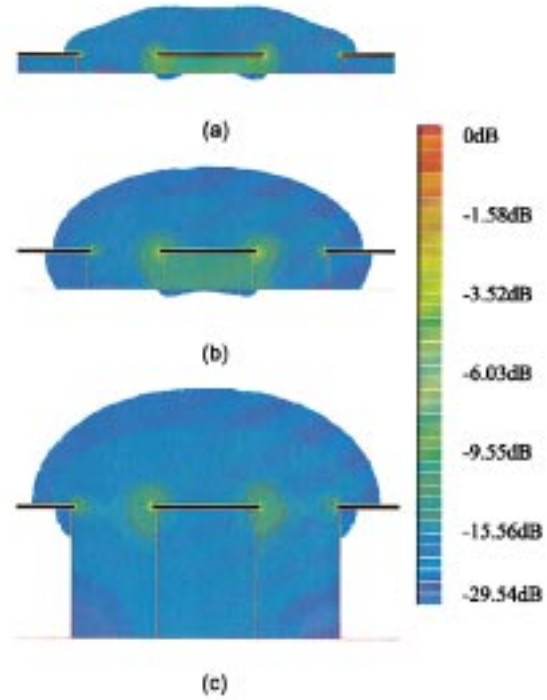


Fig. 6. Calculated electric-field magnitude for CPW lines with  $S = 50 \mu\text{m}$ ,  $W = 35 \mu\text{m}$ , and (a)  $H_p = 8 \mu\text{m}$ , (b)  $H_p = 20 \mu\text{m}$ , and (c)  $H_p = 50 \mu\text{m}$ .

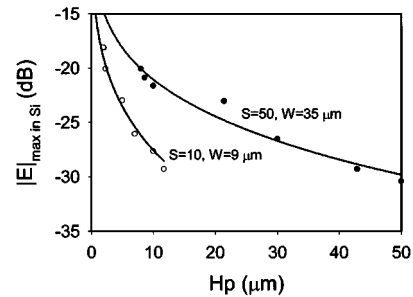


Fig. 7. Calculated maximum  $|E|$  in Si for CPW lines on polyimide interface layer after etching as a function of the polyimide thickness.

It is helpful to compare these reported characteristics with CPW lines on HRS with the same characteristic impedance. Fig. 8 shows the attenuation of a CPW line on polyimide with  $S$ ,  $W$ , and  $H_p$  of 20, 6, and  $20.15 \mu\text{m}$ , respectively, before and after polyimide etch. This line has a  $65\text{-}\Omega$  characteristic impedance after the polyimide has been etched. Two  $65\text{-}\Omega$  CPW lines on HRS are shown for comparison. First, it is seen that the CPW line on polyimide before etching has a higher attenuation than the CPW lines on HRS, and the new line presented here with the etched polyimide has significantly lower attenuation. Comparing the CPW line on polyimide after etch and the CPW line on HRS with the same center conductor width ( $S = 20 \mu\text{m}$ ), it is seen both lines have the same attenuation at low frequency, while the new line has  $1.5 \text{ dB/cm}$  higher loss at 40 GHz. However, for the two lines closer in size to each other,  $(S + 20W) = 32 \mu\text{m}$  and  $50 \mu\text{m}$  for the line on polyimide and the line on HRS respectively, the micromachined CPW has lower loss across the frequency range of 1–40 GHz.

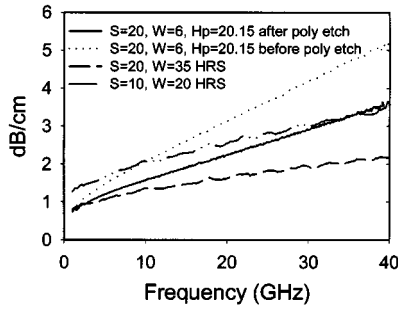


Fig. 8. Measured attenuation of CPW lines on polyimide before etch, on polyimide after etch, and on HRS with  $Z_c = 65 \Omega$ .

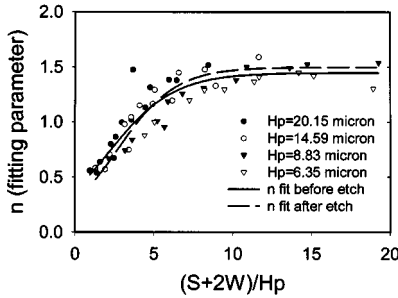


Fig. 9. Measured frequency-dependent parameter  $n$  of  $\alpha = f^n$  for CPW lines on a polyimide interface layer before etch with a curve fit of  $n$  after etch as a function of  $(S + 2W)/H_p$ .

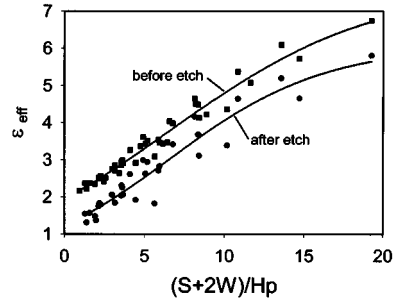


Fig. 10. Comparison of measured effective permittivity of CPW lines on Si with a polyimide interface layer before and after etching as a function of  $(S + 2W)/H_p$  (frequency = 20 GHz).

#### IV. DESIGN RULES

As was shown in Figs. 3 and 4, the attenuation of CPW lines on CMOS-grade Si is very dependent on the polyimide thickness and the strip and slot width. For low attenuation at higher frequencies, the frequency dependence  $n$  should be as small as possible. To establish a design rule,  $n < 1$  may be used. Fig. 9 shows  $n$  as a function of the CPW geometry and polyimide thickness before etching. Also shown in Fig. 9 is a regression fit of the measured data for the frequency dependence after etching. To satisfy the design rule of  $n < 1$ ,  $(S + 2W)/H_p \leq 4$  must be maintained for low attenuation. Alternatively, the measured  $\epsilon_{\text{eff}}$  may be used to determine criteria on the CPW geometry. Fig. 10 shows the measured  $\epsilon_{\text{eff}}$  of CPW lines on polyimide before and after etch. As already discussed,  $\epsilon_{\text{eff}}$  should be less than 1.9 if the field interaction with the Si is low. As shown in Fig. 10, this requires  $(S + 2W)/H_p < 3$ . Note that  $\epsilon_{\text{eff}} > 1.9$  for all linewidths before the polyimide is etched. Finally, finite-element analysis indicates that for maximum  $|E|$  in the Si to be less

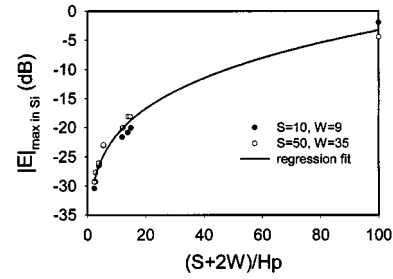


Fig. 11. Calculated maximum  $|E|$  in the Si for CPW lines on a polyimide interface layer after etching as a function of  $(S + 2W)/H_p$ .

than  $-30$  dB,  $(S + 2W)/H_p$  must be less than two, as shown in Fig. 11. Based on these three observations, a reasonable design rule for low-loss CPW lines on low-resistivity Si with an etched polyimide is  $(S + 2W)/H_p \leq 3$ .

#### V. CONCLUSION

Micromachined polyimide CPW lines on low-resistivity silicon substrates have been shown to have low attenuation and a low effective permittivity. Since it is known that CPW attenuation varies inversely with the line dimensions [12], the low attenuation of the narrow lines presented here is exciting. Therefore, this new transmission line provides Si RFIC designers using CMOS grade Si wafers another important low-cost option that is more robust and simpler to fabricate than membrane-supported lines on CMOS-grade Si [13], [14]. Furthermore, the low  $\epsilon_{\text{eff}}$  of 1.3 reported here enables high-speed circuits.

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**George E. Ponchak** (S'82–M'83–SM'97) received the B.E.E. degree from Cleveland State University, Cleveland, in 1983, the M.S.E.E. degree from Case Western Reserve University, Cleveland, OH, in 1987, and the Ph.D. from The University of Michigan at Ann Arbor, in 1997.

In July 1983, he joined the staff of the Communication Technology Division, National Aeronautics and Space Administration (NASA) Glenn Research Center, Cleveland, OH, where he is currently a Senior Research Engineer. From 1997 to 1998, and again

in 2000, he was a Visiting Lecturer at Case Western Reserve University. He is interested in the development and characterization of microwave and millimeter-wave printed transmission lines and passive circuits, multilayer interconnects, uniplanar circuits, microwave microelectromechanical (MEMS) components, and microwave packaging. He is responsible for the technical management of GaAs, InP, and SiGe MMIC development grants and contracts. In addition, he is interested in the reliability of GaAs and SiGe MMICs for space applications. He has authored and co-authored over 60 papers in referred journals and symposia proceedings.

Dr. Ponchak is a member of the International Microelectronics and Packaging Society (IMAPS). He was the recipient of the Best Paper of the 1997 International Society for Hybrid Microelectronics (ISHM'97) 30th International Symposium on Microelectronics Award.



**Alexandros Margomenos** (M'99) was born in Thessaloniki, Greece, in 1975. He received the B.Sc. degree in physics from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 1998, the M.Sc. degree in electrical engineering from The University of Michigan at Ann Arbor in 2000, and is currently working toward the Ph.D. degree at The University of Michigan at Ann Arbor.

He is currently involved in the study of isolation in three-dimensional integrated circuits. His research interests include microwave and millimeter-wave circuits, micromachining, and packaging.



**Linda P. B. Katehi** (S'81–M'84–SM'89–F'95) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1977, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles, in 1981 and 1984, respectively.

In September 1984, she joined the faculty of the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, as an Assistant Professor, and then became an Associate Professor in 1989 and Professor in

1994. She has served in many administrative positions, including Director of Graduate Programs, College of Engineering (1995–1996), Elected Member of the College Executive Committee (1996–1998), Associate Dean for Graduate Education (1998–1999), and Associate Dean for Academic Affairs (since September 1999). She has authored or co-authored 410 papers published in refereed journals and symposia proceedings and she holds four U.S. patents. She has also generated 20 Ph.D. students.

Dr. Katehi is a member of the IEEE Antennas and Propagation Society (IEEE AP-S), the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), Sigma Xi, Hybrid Microelectronics, and International Scientific Radio Union (URSI) Commission D. She was a member of the IEEE AP-S AdCom (1992–1995). She was an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION. She was the recipient of the 1984 IEEE AP-S W. P. King (Best Paper Award for a Young Engineer), the 1985 IEEE AP-S S. A. Schelkunoff Award (Best Paper Award), the 1987 National Science Foundation Presidential Young Investigator Award, the 1987 URSI Booker Award, the 1994 Humboldt Research Award, the 1994 University of Michigan Faculty Recognition Award, the 1996 IEEE MTT-S Microwave Prize, the 1997 International Microelectronics and Packaging Society (IMAPS) Best Paper Award, and the 2000 IEEE Third Millennium Medal.